Design of DUAL $V_{TH}$ SUB- DOMINO LOGIC

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Abstract - In this novel method, low power Dual Vth domino logic is designed to operate in Sub-threshold region. The dual-$V_{TH}$ domino design for sub-threshold circuit utilizes the characteristics of two different $V_{TH}$ levels to achieve maximum energy saving & speed performance. EPC (Energy Per Cycle) is lowered by 10% to 29% by dual-$V_{TH}$ design over single-$V_{TH}$ version. Power optimization is shown for the Domino mode of operation using Micro wind simulations which compares performance, power dissipation, robustness of the design and efficiency of the proposed methodology is shown in a standard 40-nm CMOS process.

Index Terms - Domino mode logic, high performance, sub-threshold region, EPC, power optimization.

I. INTRODUCTION

The dual-threshold voltage method benefits from the characteristics of low and high threshold voltages. Higher threshold voltage results in less leakage current, therefore less leakage power consumption with the sacrifice of delay. On the contrary, lower threshold voltage brings more leakage power consumption with faster speed. Dual-threshold voltage design is a common method for reducing leakage power consumption for above-threshold circuits. In this thesis, dual-threshold voltage is proven effective for reducing energy consumption per cycle (EPC) of sub-threshold circuits.

Dual-Threshold Voltage Techniques:

Threshold voltage of MOSFET technology represents the value of the gate-source voltage when the current in the MOS transistor starts to increase significantly since the conduction layer just begins to appear. The threshold voltage changes with application of different source-bulk bias voltages. The threshold voltage when bias voltage is present can be summarized in the following equation,

$$ V_{th} = V_{th0} + \gamma(\sqrt{-2\phi_F + V_{SB}} - \sqrt{2\phi_F}) \ldots (1) $$

where $V_{th0}$ is the threshold voltage with zero source-bulk bias voltage ($V$), which means that the bulk terminal is connected to ground in NMOS transistors and the bulk terminal is connected to supply voltage in PMOS transistors, $V_{SB}$ is the source-bulk bias voltage ($V$), $2\phi_F$ is the surface potential parameter ($V$), $\gamma$ is the body effect parameter ($\sqrt{V}$). Applying a positive $V_{SB}$ to an NMOS transistor or a negative $V_{SB}$ to a PMOS transistor can increase threshold voltages, which is called reverse body biasing. Applying a negative $V_{SB}$ to a NMOS transistor or a positive $V_{SB}$ to a PMOS transistor can decrease threshold voltages, which is called forward body biasing. Higher threshold voltage results in less leakage current, therefore less leakage power consumption, at the cost of larger delay. On the contrary, lower threshold voltage brings more leakage current, and therefore leakage power consumption with faster speed. By utilizing dual or multiple threshold voltages in a circuit, designers can suppress leakage current while meeting certain performance requirements as well.

II. SOURCES OF POWER DISSIPATION

Power consumption has become a primary constraint in VLSI design. Several methodologies, energy efficient algorithms, logic families has already been invented which directly addresses power reduction, with the focus rather on ever faster clock rates and logic speeds in subthreshold design technique. How to get more reduction efficiently to design a robust circuitry in subthreshold region is the main focusing area for researchers in both industry and academia. The approach which will be presented here, takes another viewpoint, in which all possible power constraints and their types of a
CMOS based system design are investigated with the goal of the reduction in the power dissipation.

**Fig.1 Main Sources of Power Dissipation in CMOS**

Power consumption is an important property of a design that affects feasibility cost and reliability. It influence a greater number of critical design decisions, such as power supply capacity, the battery lifetime, supply line sizing, packaging and cooling requirements. Fig1 shows the main constraints of power dissipation and their types in CMOS based VLSI design circuits.

### III. Challenges in Sub-threshold Design

The main goal of this section is to focus on the challenges of subthreshold logic design; the characteristics of the semiconductor behavior vary in weak inversion. The minimum power supply, frequency reduction and many others challenging parameters will be discussed in the following [15-18]

#### A. Delay: The first and preeminent challenges of the circuit operation in the subthreshold region are the longer impedance or delay relatively having lower frequency due to weak current flow in the channel.

#### B. Device Scaling: The device scaling provides great merits like reduction in gate capacitance, switching energy and gate delay. On the other hand there are some demerits like including process variability, increased subthreshold leakage, increased gate leakage at super-threshold voltages, exponential sensitivities to V\_th, V\_dd, and inverse subthreshold slope.

Transistor design is important in case of subthreshold regime and these days researchers are trying to find out how subthreshold circuits will fare under device scaling and to provide improved scaling strategies targeting the needs of subthreshold circuits. Today’s latest research area is to develop novel circuit technology to reduced subthreshold leakage current with minimum power consumption.

#### C. Exploring New Logic for Robust Design: The current ratio I\_ON/I\_OFF decreases with low V\_dd which may reduce robustness due to this reason static CMOS gates works continuous and gives better results in subthreshold but because of scaling, voltage or process variation and other arising effects CMOS offer greater resiliency. A lot of work needs to be done for exploring new logic families to design a robust subthreshold logic circuits.

#### D. PVT Variations: Process, Voltage, and Temperature (PVT) variations substantially affect the threshold voltages and frequency which causes a large variance in the behavior of subthreshold circuits, just because of exponential I-V characteristics, threshold voltage variations occurs due random dopant fluctuations and they change the properties of a transistor relative to its immediate neighbors. These signal delay variations can lead to timing violations. Therefore variability-aware design is an important challenge for robust and reliable subthreshold circuits.

#### E. Temperature: The effect of temperature variation on the circuit behavior is another important challenge, mobility degradation in the channel during strong inversion generally slow down the circuit and also rises the temperature. This arising temperature decreases threshold voltage which exponentially increases subthreshold current. In other term we can say when temperature scaling is performed the circuit gets cool down it not only increases mobility but also minimizes subthreshold leakage. Generally at low temperature gate leakage becomes the main leakage.

#### F. Advancement in Design Tools: System verification is a significant task after designing. With the advancement of technology, design tools modification must be done having the additional function like statistical distributions of delay and power, introduced by local variations so that verification of large systems running at such ultra low voltages and power dissipation estimation of circuits could be performed easily.

#### G. Noise Margin: Noise margin is directly affected from the supply voltage and degraded due to the high sensitivity to process variations and low-V\_dd subthreshold circuits. Therefore in the presence of noise special techniques must be used to design a subthreshold circuit.

#### H. Reliability Problems: Reliability failures are typically caused by marginal manufacturing defects that are not significant enough to prevent the IC from passing a production test but can cause failure under use. Test coverage problems and circuit sensitivity are always followed by reliability problem. Reliability problems are
worst kind of problems due to potentially severe consequences.

IV. Logic Operation in Sub-threshold Region

Around 1970s, with the discovery of weak inversion region of MOS transistors, researchers have confirmed that CMOS transistors can function correctly under normal and sub-threshold supply voltages. The sub-threshold current $I_{sub}$ is the main source of current in the sub-threshold region.

\[ I_{sub} = I_0 \exp\left(\frac{V_{gs} - V_{th}}{nV_t}\right) \left[1 - \exp\left(-\frac{V_{ds}}{V_t}\right)\right] \] ..(2)

Where, $I_0 = \mu Cox$ where $\mu$ is effective mobility, which is 0.067$m^2/V$ sec for n-channel device and 0.025$m^2/V$ sec for p-channel device, effective length, $V_t$ is the thermal voltage, which is 25.8$mV$ for room temperature, $V_{gs}$ is the gate-source voltage, $V_{ds}$ is the drain-source voltage, $V_{th}$ is threshold voltage and $n$ is sub-threshold slope, which is a technology determined parameter. $n$ is related to the ratio of oxide capacitance over depletion capacitance by

\[ n = 1 + \frac{C_{ox}}{C_{depletion}}. \]

It is in the range of 1 and 1.5 for modern deep sub-micron technology. The transistor current $I_{on}$ in the sub-threshold regime is exponentially dependent on $V_{th}$ and supply voltage due to which power, delay and current matching between two transistors is also exponentially dependent on $V_{th}$ and $V_{dd}$. This exponential dependence is a key challenge in designing circuits in subthreshold. Some of the parameters that are affected by this challenge are process variations, noise margins, soft errors and output voltage swings. Therefore, when designing energy optimal subthreshold circuits, these parameters play an important role. The current in the subthreshold region, also known as leakage current, is considered to be undesirable when operating the transistor in the super threshold region. However, this current is quintessential as far as subthreshold operation is concerned.

![Figure 2.1: Transistor current characteristics.](image)

V. Dual-Vth Design Framework

With the reduction of supply voltage in order to lower power consumption in VLSI circuits, threshold voltage scaling is needed to maintain circuit performance. However, low threshold voltage brings higher leakage power consumption.

In order to solve this problem multi threshold CMOS was recommended to control leakage power. It had been acceptable to use low threshold voltage devices for critical paths and high threshold devices for non-critical paths. The basic idea is to assign as many gates as possible to a high threshold voltage to reduce leakage power. Not all gates on the off-critical paths can be switched to high threshold voltage and only some gates which have sufficient slack can be switched to high threshold due to certain performance constraints.
assigning low Vth to all of the gates in the circuit, then properly selecting as many gates as possible to switch to high Vth to suppress leakage power consumption. As a result, critical-path gates are normally assigned low Vth to keep circuit with fast speed and off-critical-path gates are normally assigned high Vth to reduce leakage. However, the tricky part is that it is not appropriate to assign high Vth to every non-critical path gate since the circuit performance may be degraded significantly.

**VI. EPC REDUCTION IN DUAL VTH APPROACH**

It is estimate that the energy saving.Energy per cycle of sub-threshold circuits can be reduced by the dual-Vth approach. Energy per cycle (EPC) is the product of power and circuit performance, energy reduction should be a more appropriate criteria in dual-Vth algorithm compared to power reduction. Therefore, dual-Vth algorithm is proposed to maximize EPC reduction. optimal dual-Vth design, accurately determines an optimal high Vth level, and an optimal supply voltage Vddopt.

**VII. Dual vth Subthreshold Domino design**

Sub-domino logic is similar to conventional domino logic except the transistors are operated in sub-threshold region. Sub-domino outweighs Sub-CMOS by about 32% in terms of power consumption. The Sub-domino logic is 32% faster than sub-CMOS logic. Table III gives a comparison of various performance parameters using-Sub-CMOS and Sub-Domino. It is seen from Table III that PDP of Sub-Domino logic is 10% of Sub-CMOS logic.
Sub-threshold design is an inevitable choice for achieving ultra low-power consumption. In this paper, an overview of the sub-threshold operation of MOSFET is presented briefly. Various aspects of body biasing techniques to lower the threshold voltage in the sub-threshold region are presented. To address the issues of robustness, various logic families have been investigated. Finally, carbon nano-tubes have been identified as promising candidate in deep submicron ranges especially beyond sub-70nm transistor era to further address robustness issues. To summarize the various aspects of circuit operation in ultra-low-power regime are dealt with in a nutshell. This work shall be particularly useful for researchers in this area.

References